SPECIFICATION AMENDMENTS

Please substitute paragraphs [0004], [0035], and [0036] of the specification as published, (U.S. Application Publication No. US 2005/0183099 A1) with the following:

[0004] The CISC-based microprocessor 102 uses registers to store results of executed instructions. Each register is a set of bits of high-speed memory within the CISC-based microprocessor 102 used to hold data for a particular purpose. Each register is referred to in assembly language programs by a name such as AX (the register that contains the results of arithmetic operations in a computer processor such as an ~~Intel~~ INTEL® 80X86 processor) or SP (the register that contains the memory address at the top of the stack in various CISC-based microprocessors). Each register, in essence, is shared memory between components of the CISC-based microprocessor 102. Using registers as shared memory, one component performs a specific operation and stores the result of the specific operation in a register. In a sequential fashion, another component may then access the same register to obtain the result in the performance of other operations.

[0035] FIG. 2B illustrates a portion of components comprising an internal architecture of the ρ-based microprocessor 200 in more detail. Each component is preferably represented as a ρ process that communicates through ports (each port being visually represented by a square). There are five major components of the ρ-based microprocessor 200: register array comprising [[204]] 222, [[208]] 224, and 210; a timing and control unit 214; an arithmetic and logic unit [[206]] 226; an instruction register and

decoder 212; and bus connections to the outside world 216, 218. When the ρ-based microprocessor 200 carries out a ρ instruction, it proceeds through five general steps. First, the timing and control unit 214 retrieves the ρ instruction from memory-for example, a ρ instruction to compose two processes running in parallel. Second, the timing and control unit 214 decodes the ρ instruction into electronic signals that control the ρ-based microprocessor 200. Third, the timing and control unit 214 fetches the data (the two names that are the literalization of the two processes). Fourth, the arithmetic and logic unit [[206]] 226 performs the specific operation (the composition of the two processes by deliteralization of the two names). Fifth, the timing and control unit 214 saves the result (the composition of the two processes by literalizing the composition) into a register in the register array comprising [[204]] 222, [[208]] 224, and 210.

[0036] The ρ-based microprocessor 200 includes a variety of internal registers that are used to hold temporary data, memory addresses, instructions, and information about the status of the ρ-based microprocessor 200. For example, an instruction register 212 is used to hold instructions that the ρ-based microprocessor 200 is currently executing. Decoded instructions from the instruction register 212 control the rest of the ρ-based microprocessor 200, memory, and I/O through a timing and control unit 214 and external pins to the outside world. The instruction register 212 is a process with one or more ports that communicate with the timing and control unit 214, which is another process with its own ports. The instruction register 212 preferably communicates with an internal data bus [[202]] 220, which can also be represented as a process with its own ports. The internal data bus [[202]] 220 is used to carry information

to or from memory in I/O. Preferably, the bus lines of the internal data bus [[202]] 220 are bidirectional lines capable of transmitting information in both directions. Status registers [[208]] 224 (which also communicate through ports) include temporary registers that are used to hold information from the memory for an arithmetic logic unit [[206]] 226 (which also communicates through ports). The other input to the arithmetic logic unit [[206]] 226 is from an accumulator [[204]] 222 (using ports for communication). The status registers [[208]] 224 include a flag register that is used to indicate operations of the arithmetic logic unit [[206]] 226. The status registers [[208]] 224 also include general-purpose registers for storing information. The accumulator [[204]] 222 is used to accumulate answers after almost every arithmetic and logic operation performed by the arithmetic logic unit [[206]] 226. One can consider the accumulator [[204]] 222 to be the answer register because an answer is normally found here. Both the accumulator [[204]] 222 and the status registers [[208]] 224 are coupled to the internal data bus [[202]] 220 for transmitting and receiving information. A program counter 210 (whose communication occurs through ports) is also coupled to the internal data bus [[202]] 220. The purpose of the program counter 210 is to be used by the ρ-based microprocessor 200 to locate the next instruction to be executed. The program counter 210 allows the ρ-based microprocessor 200 to execute the next instruction from the memory. The ρ-based microprocessor 200 includes an address buffer 218 and a data buffer 216 for buffering information into and out of an address bus (not shown) and a data bus (not shown).

DRAWING AMENDMENTS

Please substitute the attached Replacement Sheets of drawings for the corresponding previously submitted drawing sheets. Applicant herein submits replacement drawings for Figures 2A, 2B, 5A, and 5B.